# A Universal DFT Verification Environment: Filling the Gap between Function Simulation and ATE Test

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*Abstract-*The DFT (Design For Testabiligy) design has become more and more complex accompanying the increasing scale of SoC (System on Chip). How to verify DFT logic completely in simulation and how to supply test patterns with high coverage to ATE (Automatic Test Equipment) test are important for post-silicon debug and yield increase. While verification methodology is evolving, innovating and entering the UVM (Universal Verification Methodology) era, DFT verification needs to keep pace to leverage the advantages of UVM, and thereby to increase test reusability, extendibility and function coverage, etc. This paper presents a general UVM-based DFT verification environment, which can be used from modular DFT verification to SoC DFT verification, and it can generate functionally equivalent STIL (Standard Test Interface Language ) test patterns for ATE test during SoC simulation. This paper also presents a method to model hierarchically networked DFT TDR (Test Data Register) at register abstract level in the UVM environment to allow test writers focus on test sequences without taking care of the details in TDR read and write operations.

# I. Introduction

In DFT (Design For Testability) domain, the test patterns running on an ATE (Automatic Test Equipment) can be categorized into two types: scan related and non-scan related. The former can be generated using ATPG (Automatic Test Pattern Generation) tools, while the latter cannot. Like other function tests, these non-scan DFT function tests are normally created by design verification engineers using languages such as SystemVerilog or C++. However, ATEs need test patterns described by STIL (Standard Test Interface Language) or other test languages.

To fill the gap, there is usually a dedicated team to transfer function simulation to ATE test environment, or alternatively in-house automation flows are developed to enforce complex rules on test writing and register specification documentation, which are specific for a given environment and difficult to migrate.

This paper provides a universal and more efficient solution by introducing a UVM (Universal Verification Methodology) based DFT verification environment that naturally generates test patterns in STIL format during simulation and can be plugged into any UVM-based environment. This method applies to other formats that ATEs need as well.

For ultra-large-scale SoC (System on Chip), IEEE 1149 protocol alone cannot satisfy DFT design requirements, so IEEE 1687 and 1500 protocols are usually adopted to enable modular and hierarchical DFT test access, leading to challenges when writing test sequences at RAL (register abstract level), as different protocol TDRs (Test Data Register) are hierarchically located in a network connected via IEEE 1687. To access a TDR, one or more levels 1687 SIBs (Segment Insertion Bit) have to be set and the length of DR (Data Register) chain varies with SIB values. The author also comes up with a general way to model complex DFT test access network.

## Structure of This Paper

This paper is divided into four parts. The first part is about how to build a UVM-based DFT verification environment that can generate STIL test patterns naturally. Then the second part will focus on the method of lifting DFT TDR to register abstract level. The third part answers how to verify that the generated STIL pattern works. The fourth part is the result discussion and conclusions.

In both of the first and second parts, the method we developed will be elaborated as follows: first, a general overview will be provided, and then the detailed implementation will be explained with reference to an example.

# II. UVM-Based DFT Verification Environment

## Idea Overview

The STIL test pattern describes test stimulus using vectors which specify pad toggle and measurement information (called STIL information hereinafter) in a time period.

A UVM test usually contains one or several sequences which are finally broken down into streams of UVM sequence items (a.k.a transactions) and passed to UVM drivers. UVM drivers are normally used for toggle and sample pads of DUT, meaning that they also contain the STIL information passing through. In fact, as to be demonstrated in this paper, the UVM drivers are the best supplier of STIL information.

With the precondition that any pad drive and sample are controlled by a UVM driver, which enforces no direct pad connection in the testbench (except for clock pads), simply by collecting all STIL information from the drivers and then writing them out according to the time stamp of STIL information, we can obtain complete test vectors of a certain UVM test when the simulation finishes.

Thus, we can divide the pads of an SoC into the following types for DFT functional simulation:

1. IEEE 1149.1 compliance on-chip TAP (Test Access Port). Hereinafter, it’s simply called JTAG (Joint Test Action Group) interface as shown in Table I, which is the most important interface for DFT design. Please note that in Table I, ***read\_not\_write*** signal is not defined in IEEE 1149.1, as it is an internal signal only used in this environment, for more description please refer to Section C.5.
2. Clock pads, which are clocks that need to toggle in DFT functional simulation. See Section D for more description.
3. Reset pads. All the reset related pads are categorized into this type.
4. Other pads. Except for type 1) to 3) above-mentioned, the remaining pads are categorized into this type. See Section E for more description.

In Fig. 1, ***jtag\_driver***, ***clock\_driver***, ***reset\_driver***,and ***pad\_driver*** correspond to the above four pad types, respectively. The ***STIL\_generator*** collects STIL information from these drivers and writes them to a STIL pattern file.

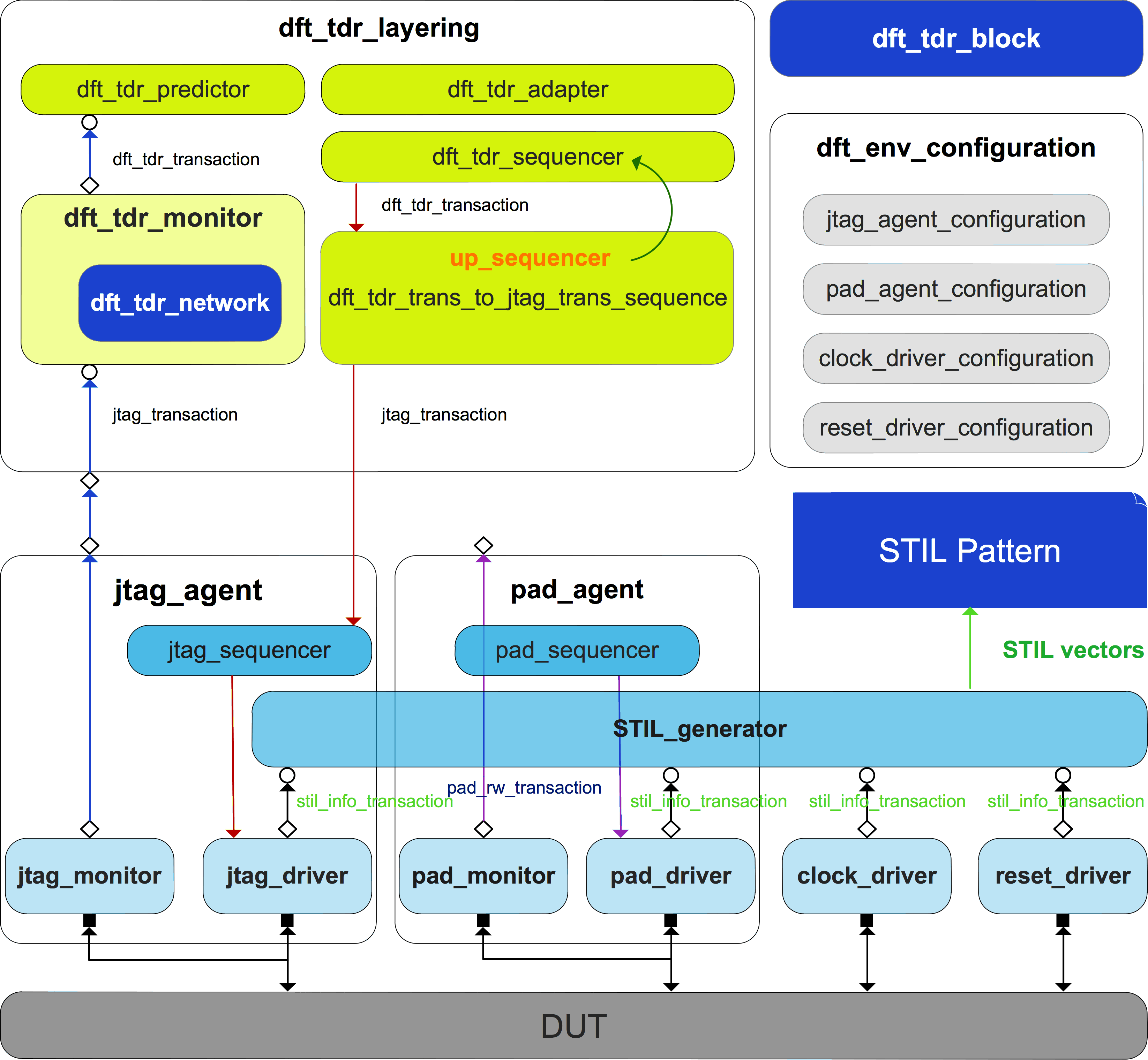


Figure 1. UVM-based DFT verification environment.

## **jtag\_agent** Implementation

In Fig. 2, ***jtag\_agent*** is composed of ***jtag\_sequencer***, ***jtag\_monitor****,* and ***jtag\_driver***, all of them configured through ***jtag\_agent\_configuration****.*

### **jtag\_agent\_configuration** Class

Fig. 3 shows properties and a key method (***pad\_info\_init*** ()) of ***jtag\_agent\_configuration*** class.

***jtag\_vi*** is virtual JTAG interface.

***reg\_block*** is TDR register model in RAL.

***gen\_stil\_file*** is configuration knob to turn on STIL pattern generation during simulation.

***stil\_file\_name*** is desired STIL pattern file name.

***pad\_name*** array stores the JTAG interface package name of an SoC and the ***pad\_dir*** array indicates pads direction. STIL pattern files need this information to describe stimuli vectors.

A DFT function test must call ***pad\_info\_init*** () method to initialize ***pad\_name*** and ***pad\_dir*** arraies before UVM ***main\_phase*** objection and store it in a configuration database for drivers and ***STIL\_generator*** fetch.

Table I

jtag Interface Definition

|  |  |
| --- | --- |
| **JTAG Interface** | |
| **Pad Direction** | Pad Name |
| **input** | TCK |
| **input** | TMS |
| **input** | TRST\_L |
| **input** | TDI |
| **output** | TDO |
| **input** | read\_not\_write |

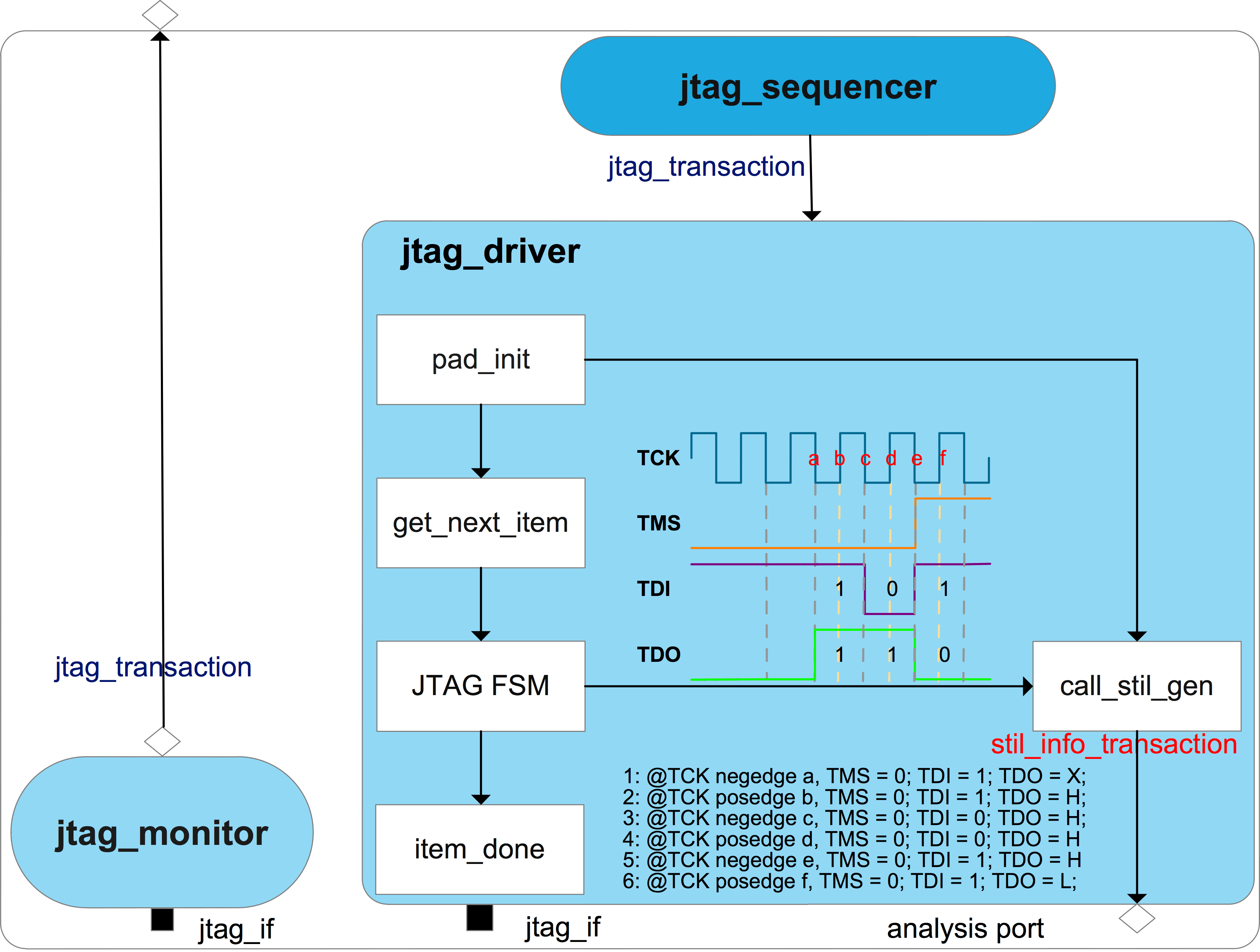


Figure 2. ***jtag\_agent*** block diagram.

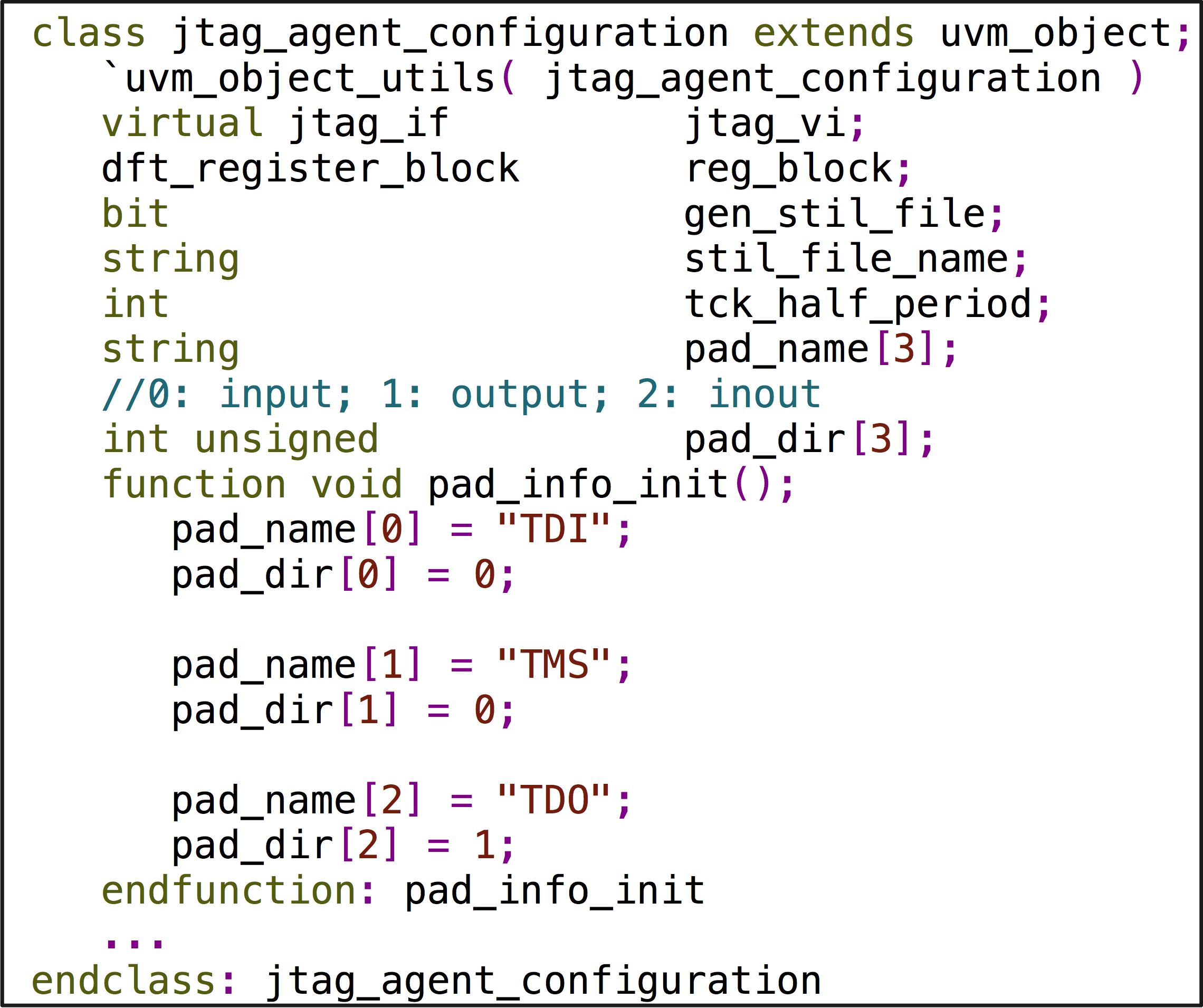


Figure 3. ***jtag\_configuration*** properties and ***pad\_info\_init*** () method

### **jtag\_transaction** Class

Fig. 4 shows properties of ***jtag\_transaction*** class.

***o\_ir*** is a dynamic array to store instruction operation code (a.k.a OPCODE) sending to DUT’s IEEE 1149.1 FSM IR (Instruction Register) and ***o\_ir\_length*** is its size.

***o\_dr*** is a dynamic array to store data sending to DUT’s IEEE 1149.1 FSM DR (Data Register) and ***o\_dr\_length*** is its size.

***tdo\_dr\_queue***, ***tdo\_ir\_queue***, ***tdi\_dr\_queue***, and ***tdi\_ir\_queue*** store data during shift IR or DR state monitored by ***jtag\_monitor***.

***chk\_ir\_tdo*** and ***chk\_dr\_tdo*** are flags to indicate ***jtag\_driver*** whether to check TDO cycle-by-cycle during shift IR or DR state.

***exp\_tdo\_dr\_queue*** is golden data expecting DUT output during shift DR state, which is used by ***jtag\_driver*** to check TDO data on the fly.

***exp\_tdo\_dr\_mask\_queue*** indicates which bit in ***exp\_tdo\_dr\_queue*** need not to check.

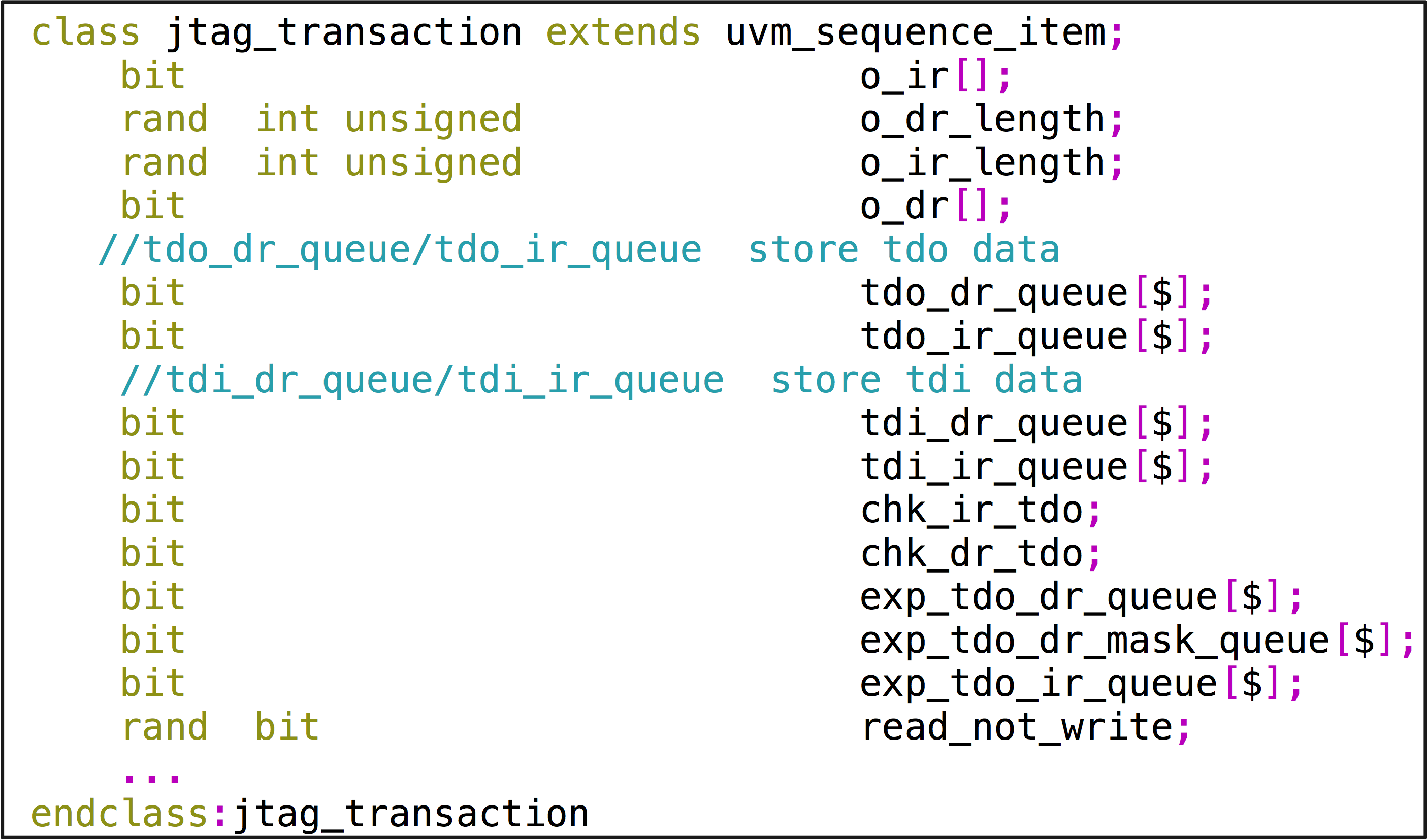


Figure 4. ***jtag\_transaction*** properties definition.

***exp\_tdo\_ir\_queue*** is golden data expecting DUT output during shift IR state, which is used by ***jtag\_driver*** to check TDO data on the fly.

***read\_not\_write*** is a flag indicating ***jtag\_monitor*** whether it’s a read or write operation for current transaction. Please see Section C.5 for more details.

### JTAG Interface Connection in Testbench

This paper categorizes pads of an SoC into four types which are driven by different drivers, so the JTAG interface shown in Table I is driven by ***clock\_driver***, ***reset\_driver***, and ***jtag\_driver*** as shown in Fig. 5.

Fig. 6 is ***jtag\_if*** definition that does not contain all signals shown in Table I because of the categorization of pads. The rest signals’ definition are defined in ***clock\_if*** and ***reset\_if*** interfaces.

### **jtag\_driver** Class

IEEE 1149.1 protocol is implemented in ***jtag\_driver***, which fetches every ***jtag\_transaction*** sequence item from ***jtag\_sequencer***, drives the JTAG interface’s TDI and TMS, and samples TDO if ***chk\_ir\_tdo*** or ***chk\_dr\_tdo*** flag is on. ***exp\_tdo\_dr\_queue*** and ***exp\_tdo\_ir\_queue*** store the expected golden value, which also will be used as the golden measure information for TDO in the generated STIL pattern.

If the ***gen\_stil\_file*** knob is on, ***jtag\_driver*** not only needs to drive and sample pads – it also converts such information to STIL information (handled by ***call\_stil\_gen*** () method), and then sends it to ***STIL\_generator*** through an analysis port, which is an object of ***uvm\_analysis\_port*** class specialized with ***stil\_info\_transaction*** type.

In Fig. 2, let us suppose ***jtag\_driver***’s FSM is in shift DR state and it is going to shift three bits 101 to DUT and sample TDO data during shift operation. The golden TDO data is three bits 110.

At TCK negative edge a, ***jtag\_driver*** keeps TSM low to let DUT’s FSM stay in shift DR state and drives TDI high to send out the first bit out. ***call\_stil\_gen*** () method converts this information as shown in line 1.

At TCK positive edge b, ***jtag\_driver*** samples TDO and compares it with the golden value, which is one bit 1. ***call\_stil\_gen*** () method converts this information as shown in line 2.

At TCK negative edge c, ***jtag\_driver*** keeps TSM low to let DUT’s FSM stay in shift DR state and drives TDI low to send out the second bit out. ***call\_stil\_gen*** () method converts this information as shown in line 3.

At TCK positive edge d, ***jtag\_driver*** samples TDO and compares it with the golden value which is one bit 1. ***call\_stil\_gen*** () method converts this information as shown in line 4.

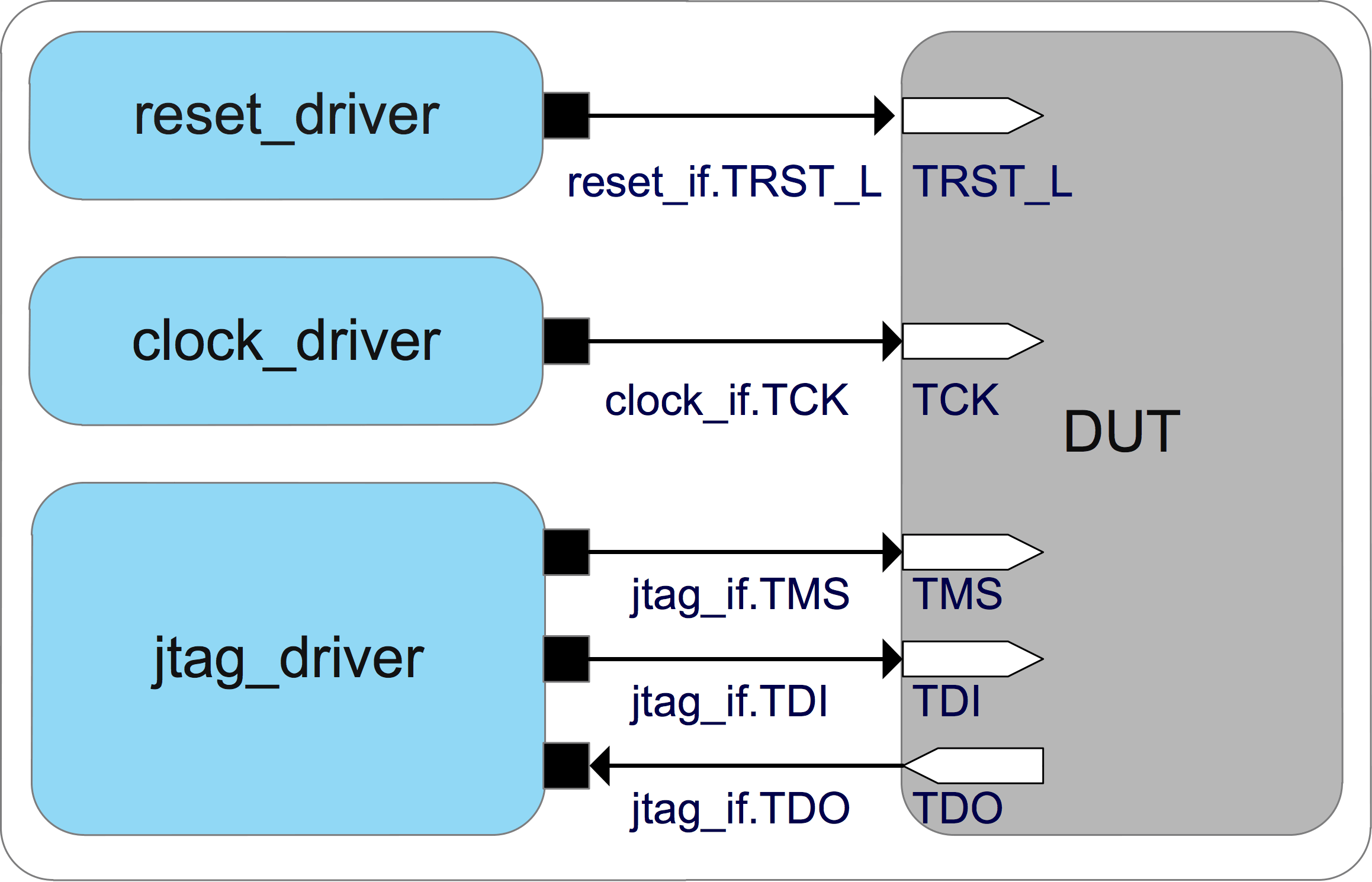


Figure 5. JTAG interface toplevel connection.

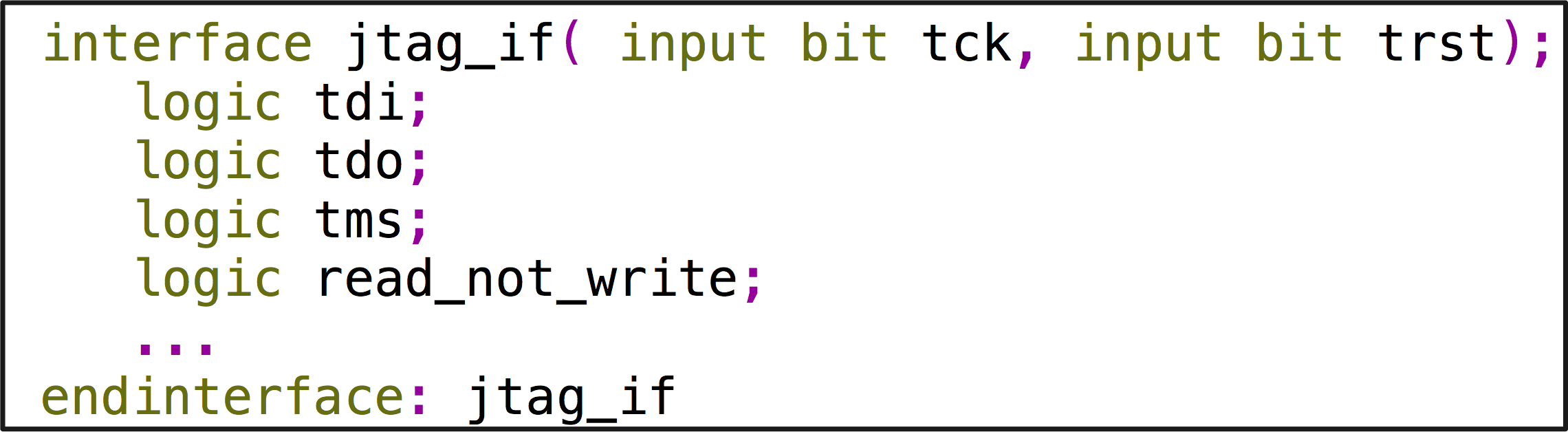


Figure 6. Signals defined in ***jtag\_if***  interface.

At TCK negative edge e, ***jtag\_driver*** drives TSM low to let DUT’s FSM go to exit1 DR state and drives TDI high to send out the last bit out. ***call\_stil\_gen*** () method converts this information as shown in line 5.

At TCK positive edge f, ***jtag\_driver*** samples TDO and compares it with the golden value which is one bit 0. ***call\_stil\_gen*** () method converts this information as shown in line 6.

### **jtag\_monitor** Class

There is a signal called ***read\_not\_write*** defined in JTAG interface shown in Table I, which is only used by ***jtag\_monitor*** to indicate whether the current transaction is a write operation or read operation.

JTAG interface is a serial bus, while shifting TDI to a register, data stored in it is being shift out on TDO, so there is not a really so-called write or read operation.

Here, we define write operation and read operation in concept for register abstract level convenience.

Read operation: data being shifted in a register is the same as the data stored in it.

Write operation: data being shifted in a register is different with the data stored in it.

***jtag\_monitor*** monitors JTAG interface activity, sampling TDI or TDO according to ***read\_not\_write*** signal, composing ***jtag\_transaction*** sequence items and then passing them to ***dft\_tdr\_laying*** as shown in the blue arrows of Fig. 1.

## Clock Pads Connection in Testbench

In STIL pattern file, the ***Timing*** block defines sets of “***WaveformTable***s”. Each ***WaveformTable*** defines the waveforms to be applied to each signal used in a vctor[1]. Because DFT function tests only use JTAG interface to configre TDRs, we define one ***WaveformTable*** in the generated STIL pattern file and use TCK’s half period as ***WaveformTable***’s ***Period***. For other clocks descirbe it as the same frequency as TCK in STIL pattern file and connect them with desired frequency form ATE during post-silicon test. So ***clock\_driver*** only need to drive TCK during simulaiton and other clocks are generated from testbech (This is the only exception that clock pads are allowed to drive from testbench in this enviroment).

Fig. 7 is an example of how to drive clocks in this DFT verification environment.

Suppose a DUT has two PLL reference clocks and a bypass clock, which need active during simulation, named as PLL1\_REF, PLL2\_REF, and BYPASS\_CLK as shown in Fig. 7.

***clock\_gen*** module in toplevel takes charge of these three clocks’ toggle. TCK of JTAG interface is generated by ***clock\_driver***.

If ***gen\_stil\_file*** knob is on, ***clock\_driver*** needs to pass TCK drive information to the ***call\_stil\_gen*** () method at the same time it drives TCK, and ***call\_stil\_gen*** () method uses the TCK drive information as all active clocks’ drive information and pass STIL information to ***STIL\_generator***.

For an ATE test, PLL1\_REF, PLL2\_REF, and BYPASS\_CLK toggle information in the STIL pattern can be regarded as a placeholder to make post silicon engineers aware that these three clocks are reference clocks, so that they will not use the toggle information described in STIL patterns to driver reference clocks, but use clocks supplied by ATE with desired frequency.

## **pad\_agent** Implementation

Fig. 8 shows componets in ***pad\_agent*** and the execution flow in ***pad\_driver*** which featches ***pad\_rw\_transaction*** from ***pad\_sequencer***.

The pad type 4) defined in Section B, can be subgrouped according to their function or interface protocol. Take memory pads, GPIO pads, and scan control pads as examples, each of them could be put in a separate subgroup.

Fig. 9 is an example of defining pad\_if using subgroups.

In Fig. 8, ***pad\_init*** () method initializes all subgroups pads in turn at the beginning of ***run\_phase*** task, and ***call\_stil\_gen*** () method converts this information to STIL information and writes to ***STIL\_generator*** through an analysis port.

Fig. 10 displays all properties of ***pad\_rw\_transaction*** class.

***grp\_num*** is used to indicate ***pad\_dirver*** which group of pads to drive.

***in\_data\_queue*** stores data being driven by ***pad\_driver***.

***out\_data\_queue*** stores data being sampled by ***pad\_driver***.

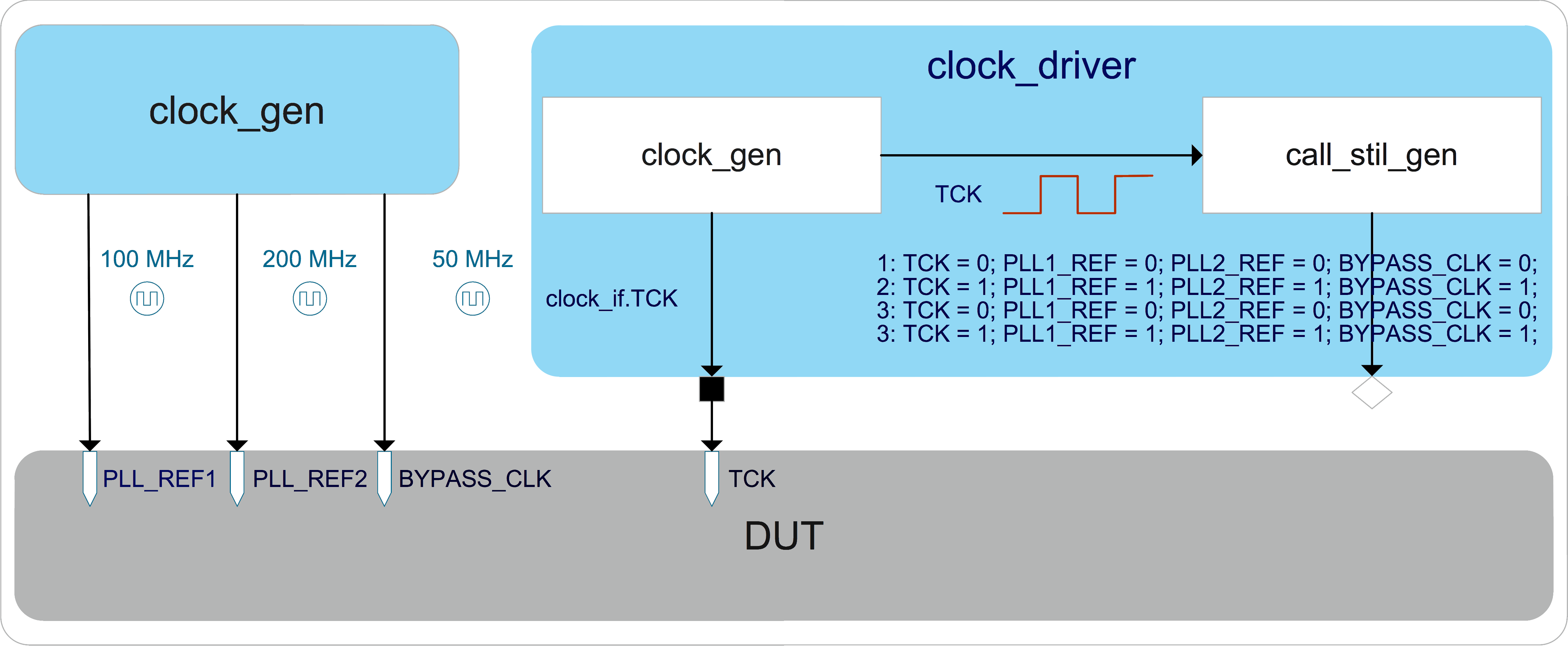


Figure 7. An example of clock pads connection in testbench.

***inout\_data\_queue*** stores data being driven or sampled by ***pad\_driver***. An unknown bit in the queue indicates ***pad\_driver*** the corresponding pad is in output mode and it will write the sampled value into the same location.

***exp\_out\_data\_queue*** and ***exp\_inout\_data\_queue*** stores golden value to let ***pad\_driver*** check on the fly and also the information for STIL pattern to measure pad value during a time period converting by ***call\_stil\_gen*** function.

Please note these queue types should be logic instead of bit to store four state values.

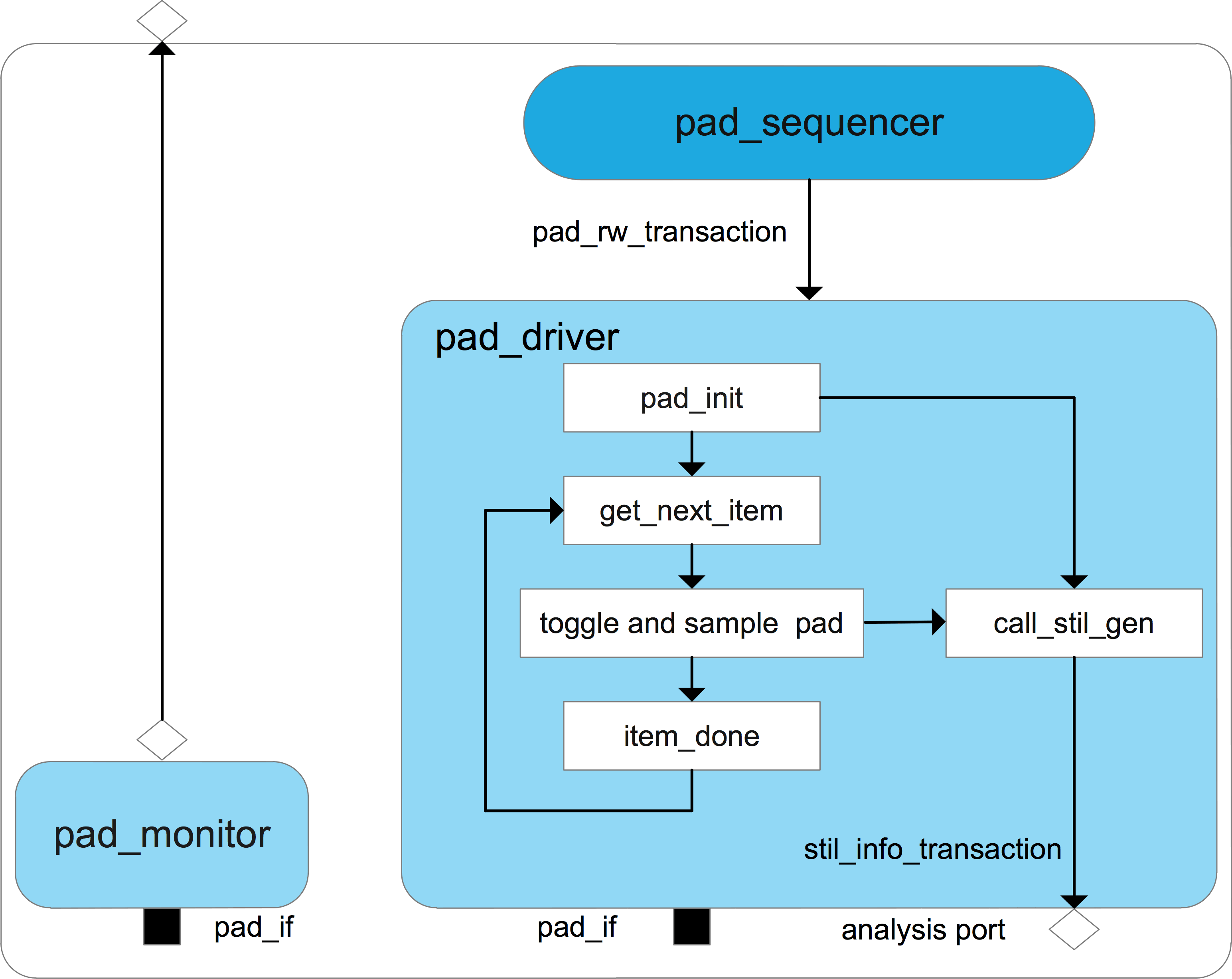


Figure 8. ***pad\_agent*** block diagram.

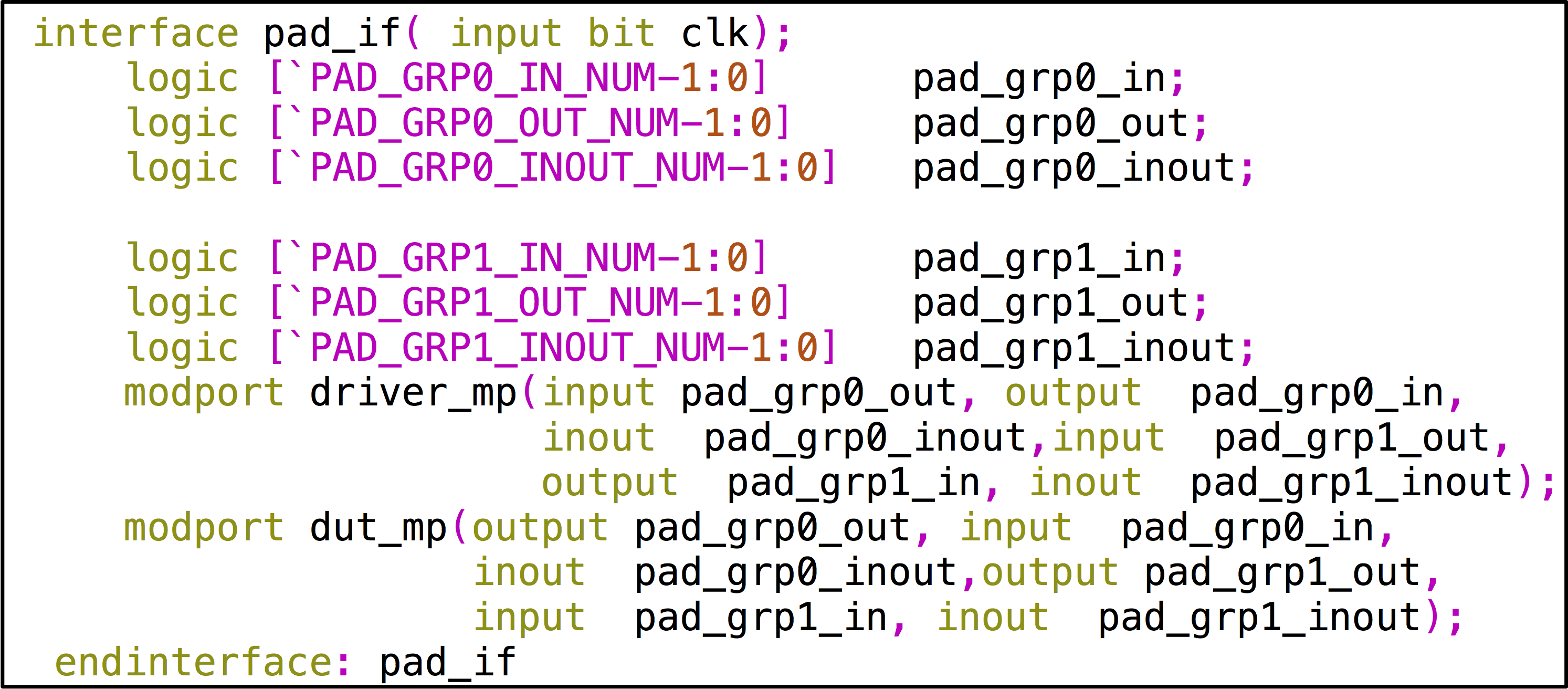


Figure 9. An example of defining ***pad\_if*** in subgroups.

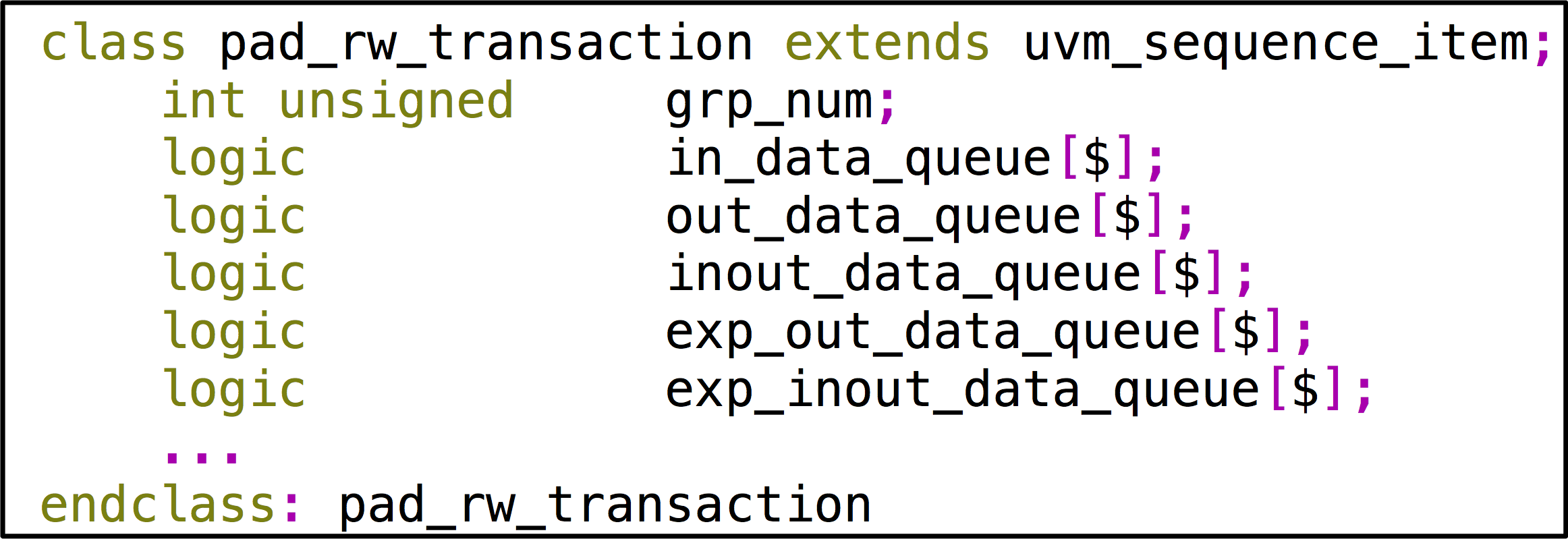


Figure 10. ***pad\_rw\_transaction*** properties definition

### **pad\_agent\_configuration** Class

Fig. 11 is an example of ***pad\_agent\_configuration*** class, which has two subgroups of pads.

A DFT test needs to initialize every group’s package name by calling the ***pad\_info\_init*** () method before the ***main phase*** objection and stores it in configuration database for ***pad\_driver*** and ***STIL\_generator*** fetch.

## **reset\_driver** Class

Fig. 12 is an example of ***reset\_driver*** that drives all resets signals defined in reset interface and call\_stil\_gen () method converts drive infomation to STIL information and writes to ***STIL\_generator*** through an analysis port.

## **STIL\_generator** Implementation

The ***stil\_generator***, which extends from ***uvm\_subscriber*** class specialized with ***stil\_info\_transaction*** type, has four analysis exports to connect with ***clock\_driver***, ***reset\_driver***, ***pad\_driver***, and ***jtag\_driver***’s analysis port separately. Since the ***uvm\_subscriber*** class has only one built-in analysis export, the ***uvm\_analysis\_imp\_decl*** macro needs to be used to declare analysis imp export and its associated ***write*** () method for the remaining analysis export [2].

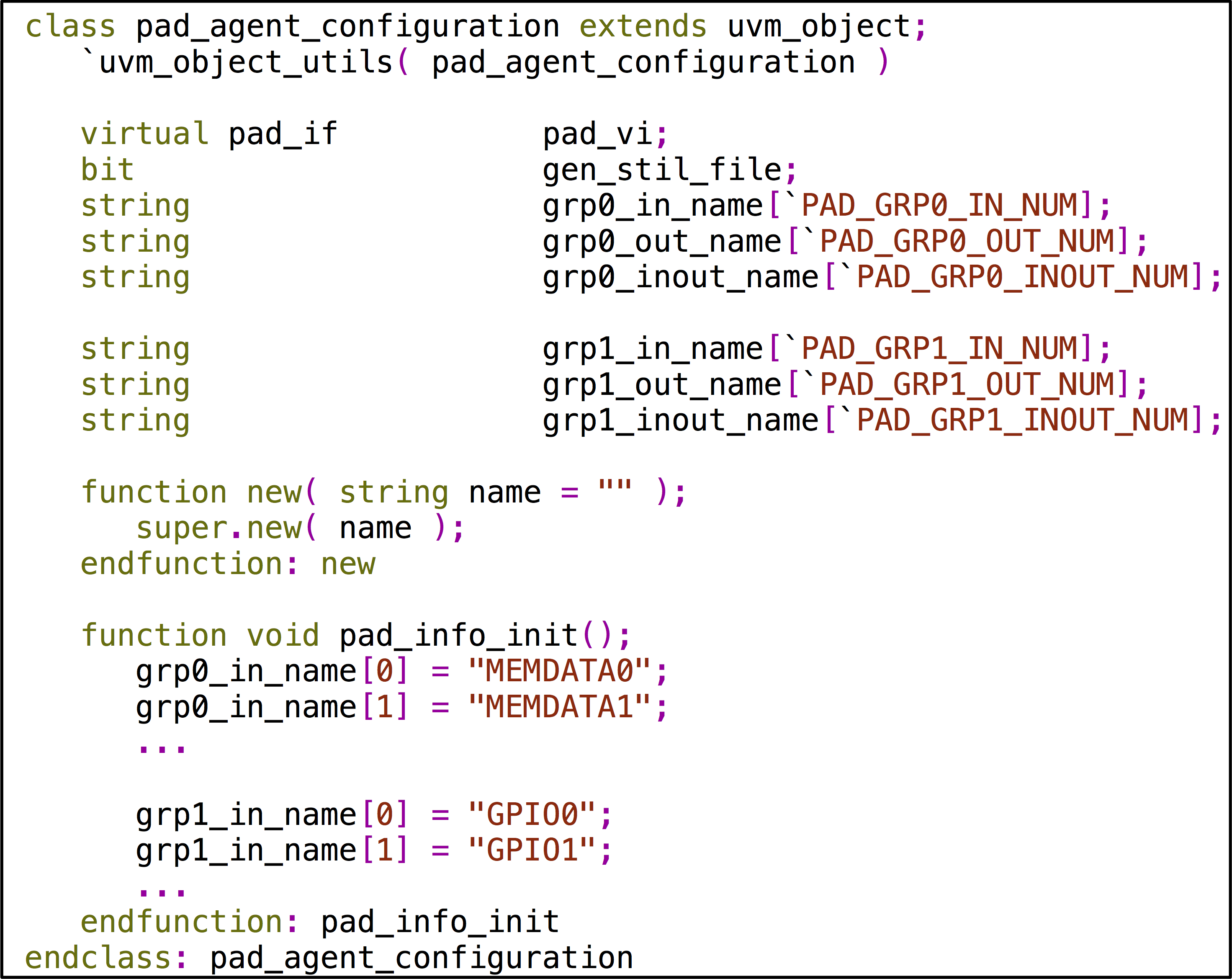


Figure 11. ***pad\_agent\_configuration*** properties definition example

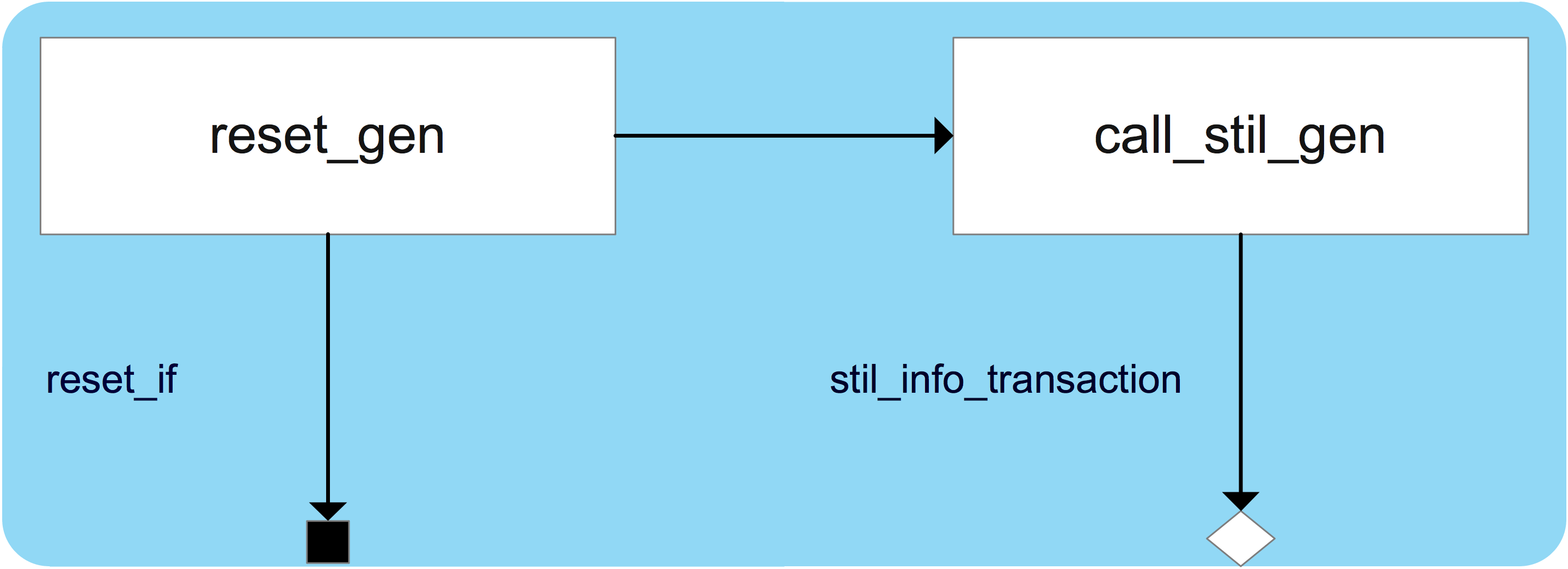


Figure 12. An example of ***reset\_driver***.

***stil\_info\_transaction*** is defined in Fig. 13. ***stil\_info*** is pads drive and measure information and ***comment info*** is the comment going to be printed out with the ***stil\_info***.

In Fig. 14, each driver’s analysis port has its corresponding ***write*** () method, a semaphore which has only one key and a group of ping-pong buffers which have two variables, called ***ping\_data\_rdy*** and ***pong\_data\_rdy,*** to indicate ping-pong buffer status.

The ***stil\_info\_transaction*** written through a driver’s analysis port is stored in a ping-pong buffer group, each buffer stores one ***stil\_info\_transaction***.

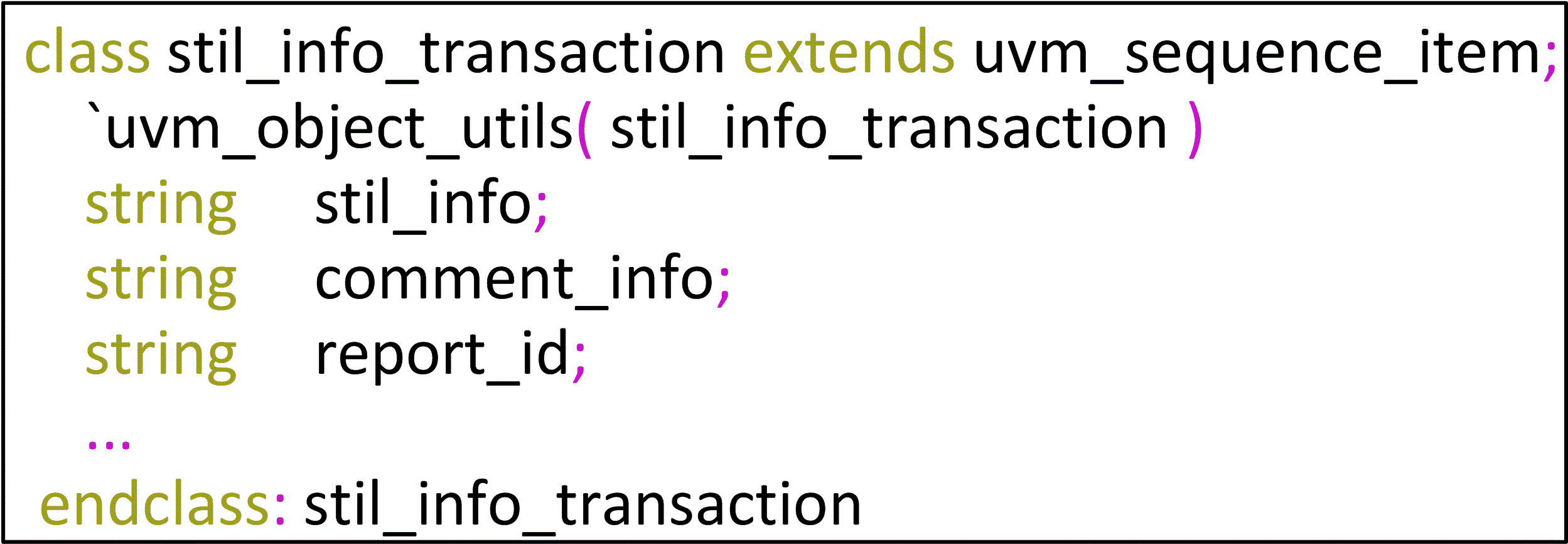


Figure 13. ***stil\_info\_transaction*** properties.

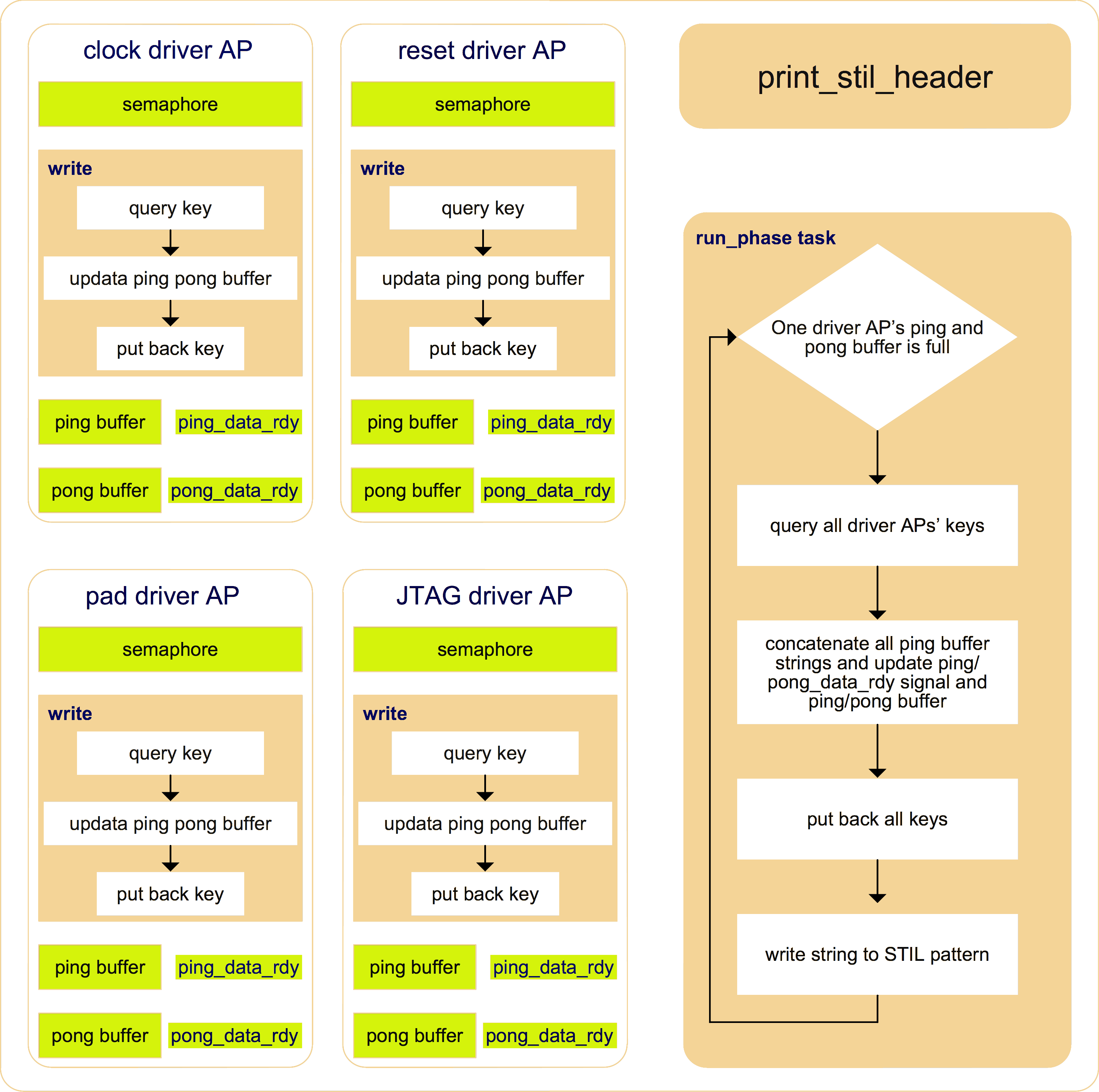


Figure 14. ***STIL\_generator*** block diagram.

The ***STIL\_generator*** needs to collect all ***stil\_info\_transaction*** coming from the same simulation time slot, to concatenate ***stil\_info*** of every ***stil\_info\_transaction***, and to write them out as a single test vector. To make sure ***stil\_generator*** does not miss any ***stil\_info\_transaction*** from the same time slot, it has to suspend the ***run\_phase*** task in ***stil\_generator*** until all other ***run\_phase*** tasks finish. However, in UVM, because all ***uvm\_component*** ***run\_phase*** tasks are executed in parallel and the ***stil\_generator*** itself is an ***uvm\_component***, there is no easy way to schedule the simulation events in ***stil\_generator***’s ***run\_phase*** task to be executed after all other drivers’ ***run\_phase*** task events finish.

To resolve this issue, a group of ping-pong buffers is introduced. The ***write*** () method always writes the ping buffer first and then the pong buffer, so the ping data and pong data come at different simulation time slots. Once a group of ping-pong buffers is full, which indicates the simulation has already moved forward, it will be the right time to collect all ping buffer data and write them out.

The ***run\_phase*** task of ***stil\_generator***, as shown in Fig. 14, always checks if a driver’s ping-pong buffer group is full. If the result is true, it will query each key of the semaphore belonging to the corresponding driver. Once it gets all the keys, it will then fetch all ping buffer data, update the ping-pong buffer groups (if both ping and pong buffers are empty, do nothing; if the ping buffer is full and pong buffer is empty, clear ***ping\_data\_rdy***; if both ping and pong buffers are full, copy the pong buffer data to the ping buffer and clear ***pong\_data\_rdy***), and put back all keys and write a test vector to STIL pattern.

# III. DFT TDR Abstraction

## Idea Overview

For ultra-large-scale SoC, usually there is a group of TDRs, which are either IEEE 1500 or IEEE 1149.1 compliance, being used to configure the DFT design of a tile or a large design block. The TDR groups among different tiles are chained together using IEEE 1687 protocol. Fig. 15 is an example of DFT TDR access network.

It is necessary to level up TDR access in RAL, so as to make it easy to migrate UVM tests developing from this UVM-based DFT verification environment among verification environments and tests from block to system levels. By doing this test writers can focus on test sequences as such, rather than the complex operation of accessing every TDR hierarchically located in the network.

For non-UVM-based environment, the normal way is to define a base class according to its protocol (for example, to define an IEEE1500 TDR base class and an IEEE 1149 TDR base class) and wrap up a TDR access operation inside its extension. When DFT access network changes, the wrapped-up access operation in each TDR class has to be updated accordingly. Such work is usually time-consuming. However, the method of modelling DFT TDR in UVM-based environment is rarely seen in literature to the author’s knowledge.

This paper presents a neat and easy maintainance way to abstract TDR in UVM-based environment, as shown in Fig. 16.

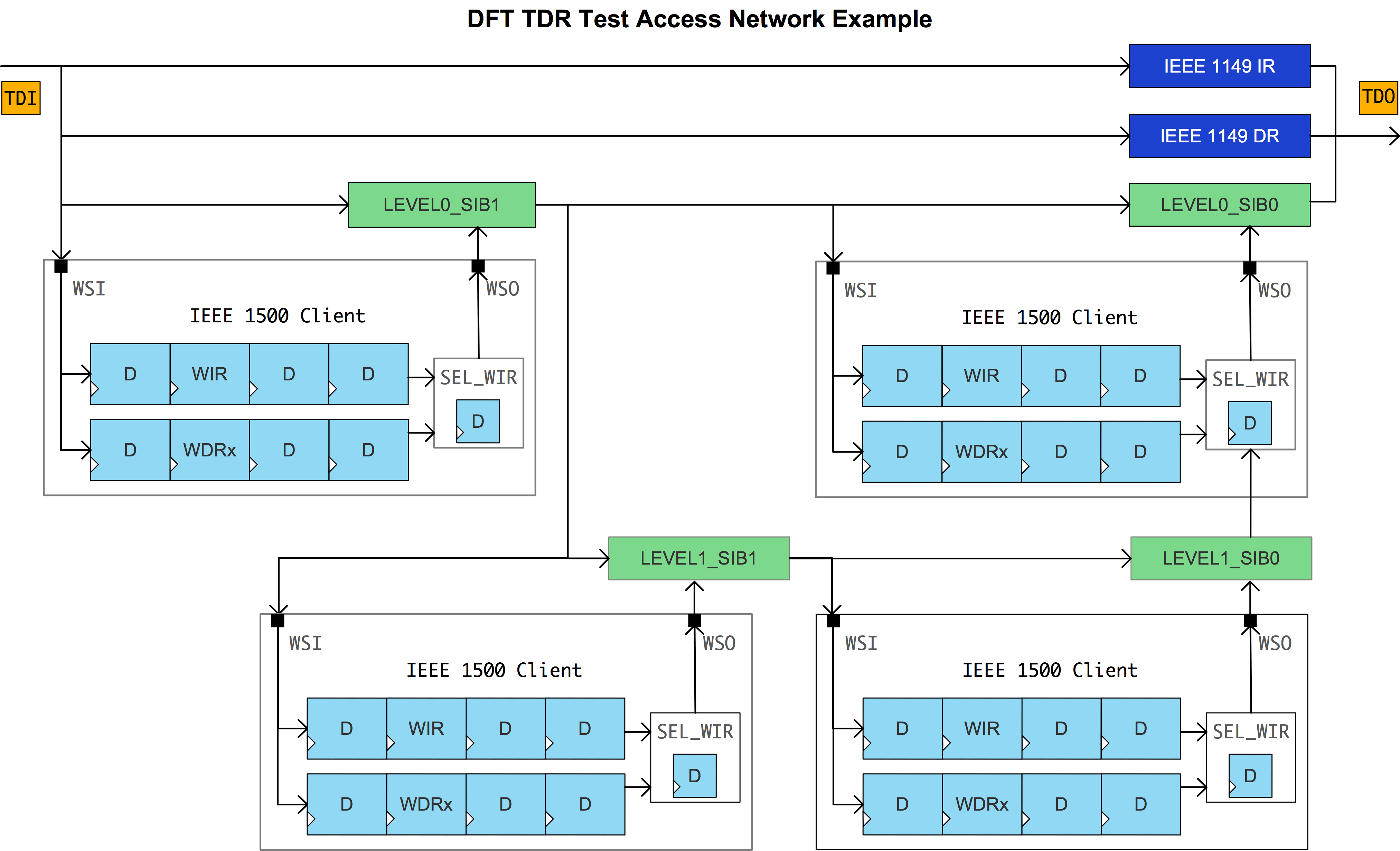


Figure 15. DFT TDR access network example.

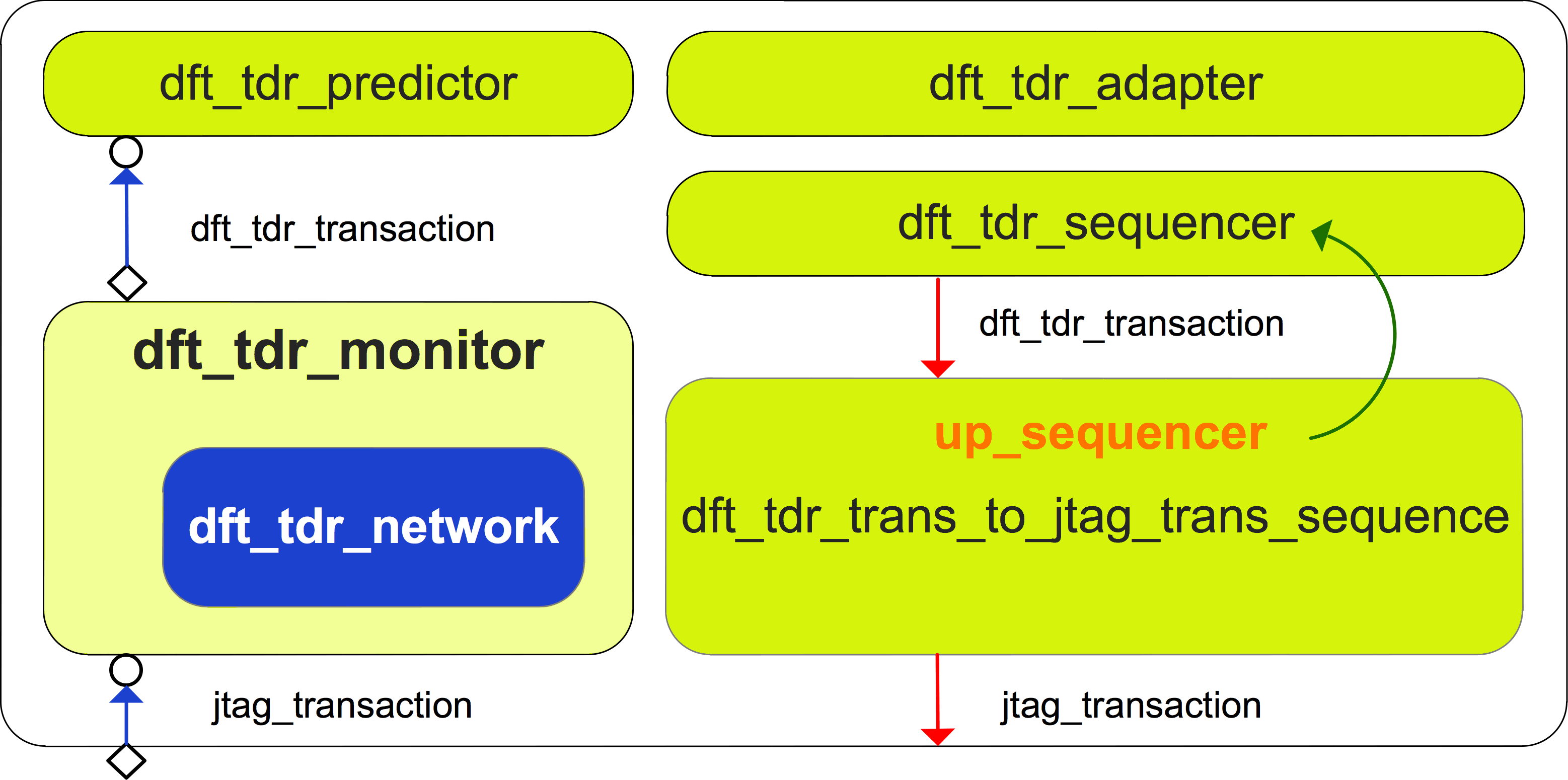


Figure 16. ***dft\_tdr\_layering*** block diagram.

We can encode a TDR’s location information into its address as shown in Fig. 17 and model an equivalent TDR access network named as ***dft\_tdr\_network*** in ***dft\_tdr\_monitor*** as shown in Fig. 16.

In Fig. 1, the reg2bus direction is shown in red lines, where ***dft\_tdr\_trans\_to\_jtag\_trans\_sequence*** fetches ***dft\_tdr\_transaction***s, unpacks address, decodes SIB code, and then generates ***jtag\_transaction***s to ***jtag\_sequencer*** [3]. For the bus2reg direction shown in blue lines, ***dft\_tdr\_network*** maintains network status using ***jtag\_transactions*** from ***jtag\_monitor***. When ***sib\_node***s value hit SIB code in ***dft\_tdr\_block***, ***dft\_tdr\_monitor*** writes a ***dft\_tdr\_transaction*** to ***dft\_tdr\_predictor***.

In this way, the TDR class definition is very neat, and only needs to declare each bit field. Fig. 19 is an example of a TDR class definition. When TDR access network changes, we only need to update ***dft\_tdr\_network*** and ***dft\_tdr\_trans\_to\_jtag\_trans\_sequence***, while all TDR class definitions don’t need any update which can save a lot of test environment setup time.

## DFT TDR Access Network Modelling

In DFT TDR access network, a SIB bit and a TDR bit can be modelled as shown in Fig. 18.

***out\_update*** () method is to model the active clock edge triggering the shift register bit during shift operation and ***value\_update*** () method is to model the active clock edge triggering the update register bit during update operation.

***dft\_tdr\_network*** usese ***sib\_node*** and ***reg\_node*** to construct an equivalent network as DUT.

And it only needs to model each 1500 client’s IR and a WDR whose length is dynamic, which can calculate from ***jtag\_transaction*** coming from ***jtag\_monitor*** and current network chain length. It need not actually model every TDR, because each time only a TDR can be configured in a 1500 client.

## DFT TDR Class Definition

DFT TDR class definition is similar to other function registers, which extend from ***uvm\_reg*** class. A bypass TDR which has only one bit field is defined in Fig. 19 as an example.

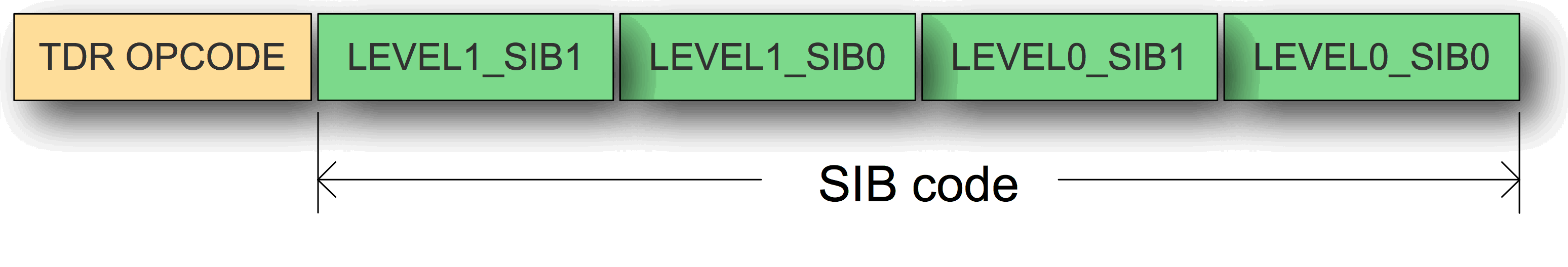


Figure 17. TDR address encode.

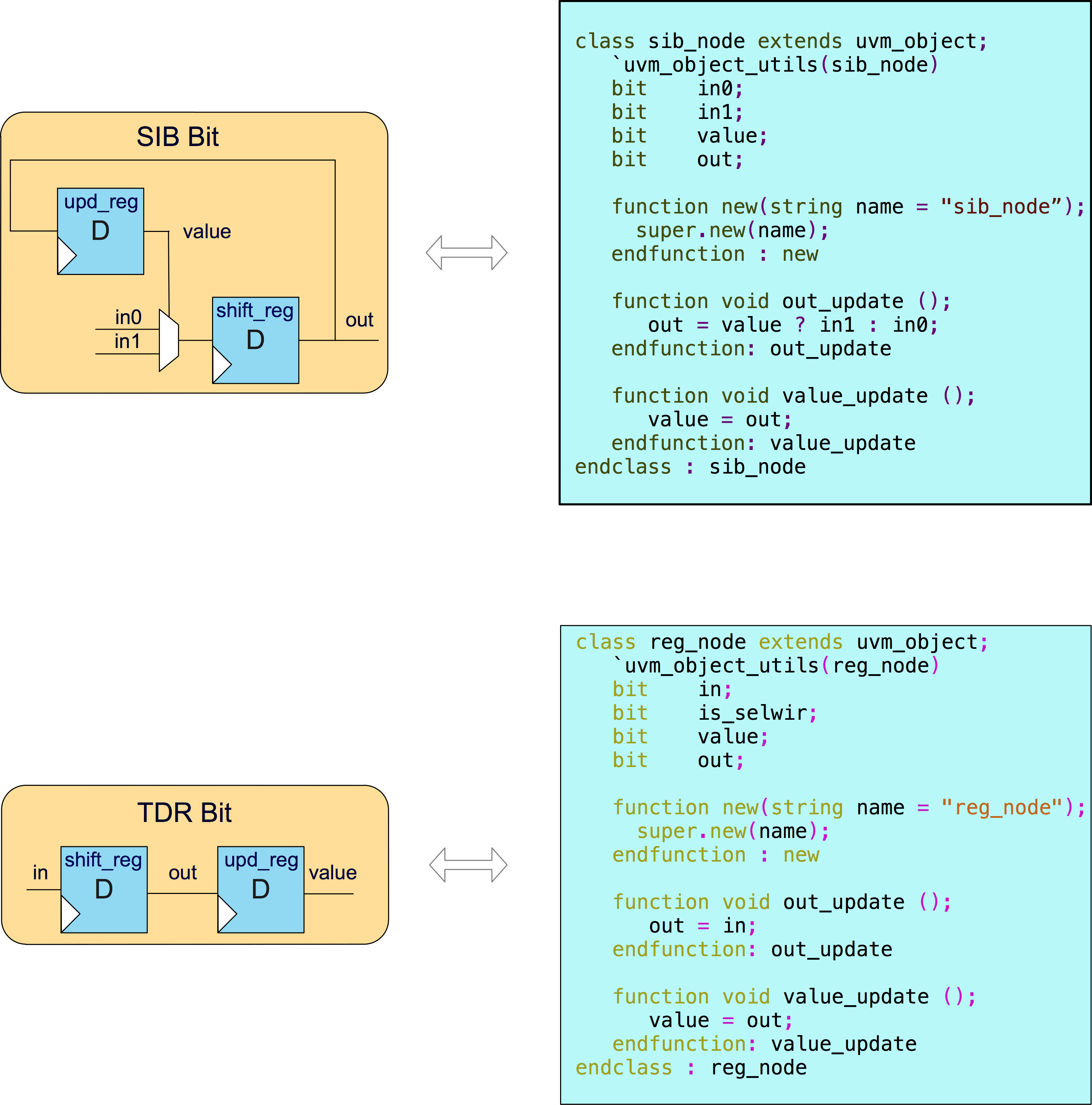


Figure 18. TDR access network element modelling.

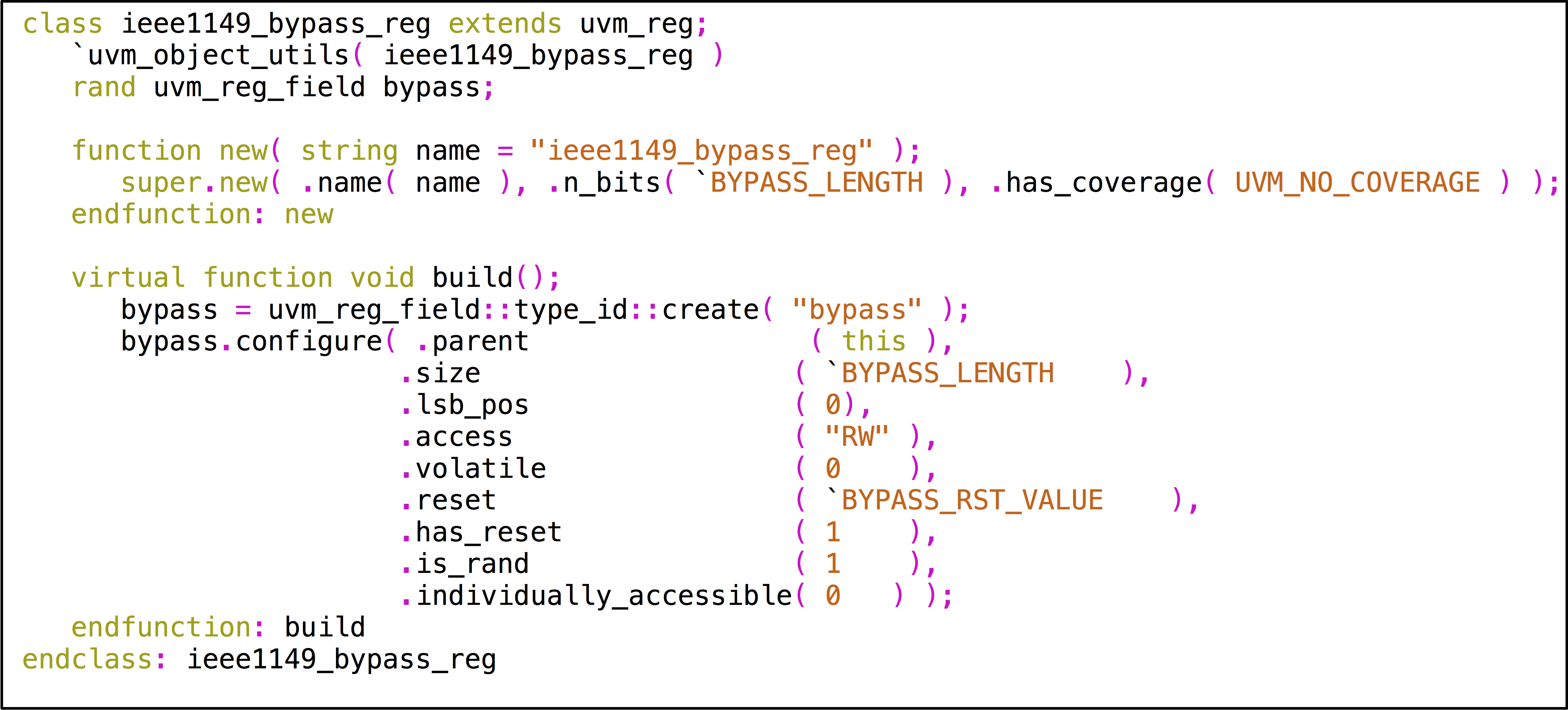


Figure 19. DFT TDR definition example.

## **dft\_tdr\_transaction** Class and **bus\_reg\_ext** Class

***bus\_reg\_ext*** class is used for sending golden value to ***jtag\_driver*** when doing register read or write in RAL. ***dft\_tdr\_adpter*** colons the extension information to the handle of extension in ***dft\_tdr\_transaction*** in bus2reg direction.

Fig. 20 and Fig. 21 show all properties of ***dft\_tdr\_transaction*** and ***bus\_reg\_ext*** class.

***read\_not\_write*** indicates current register operation is a ***UVM\_READ*** or ***UVM\_WRITE*** kind.

***address*** is the encoded TDR address.

If current register access kind is ***UVM\_WRITE***, ***dft\_tdr\_adapter*** shift write data to ***wr\_data\_q***. If current register access kind is ***UVM\_READ***, ***dft\_tdr\_adapter*** shift the default value of the register to ***wr\_data\_q***.

***extension*** is an object of ***bus\_reg\_ext*** class, which is used to transfer the side information for TDO pad checking in RAL.

***reg\_length*** stores current register’s length.

In bus2reg direction, if current register access kind is ***UVM\_WRITE***, ***dft\_tdr\_adapter*** returns data in ***wr\_data\_q*** else returns data in ***rd\_data\_q***.

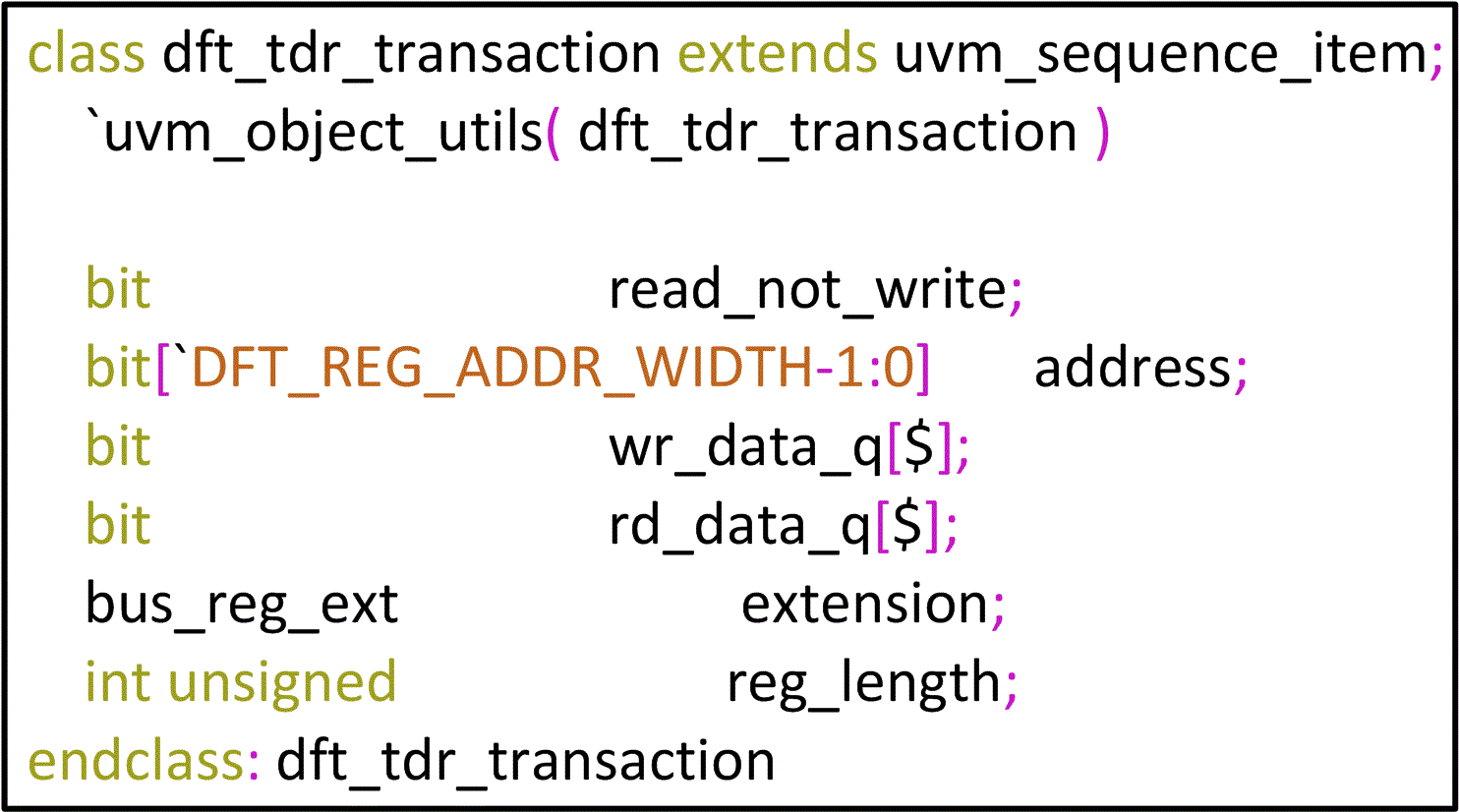


Figure 20. ***dft\_tdr\_transaction*** properties definition.

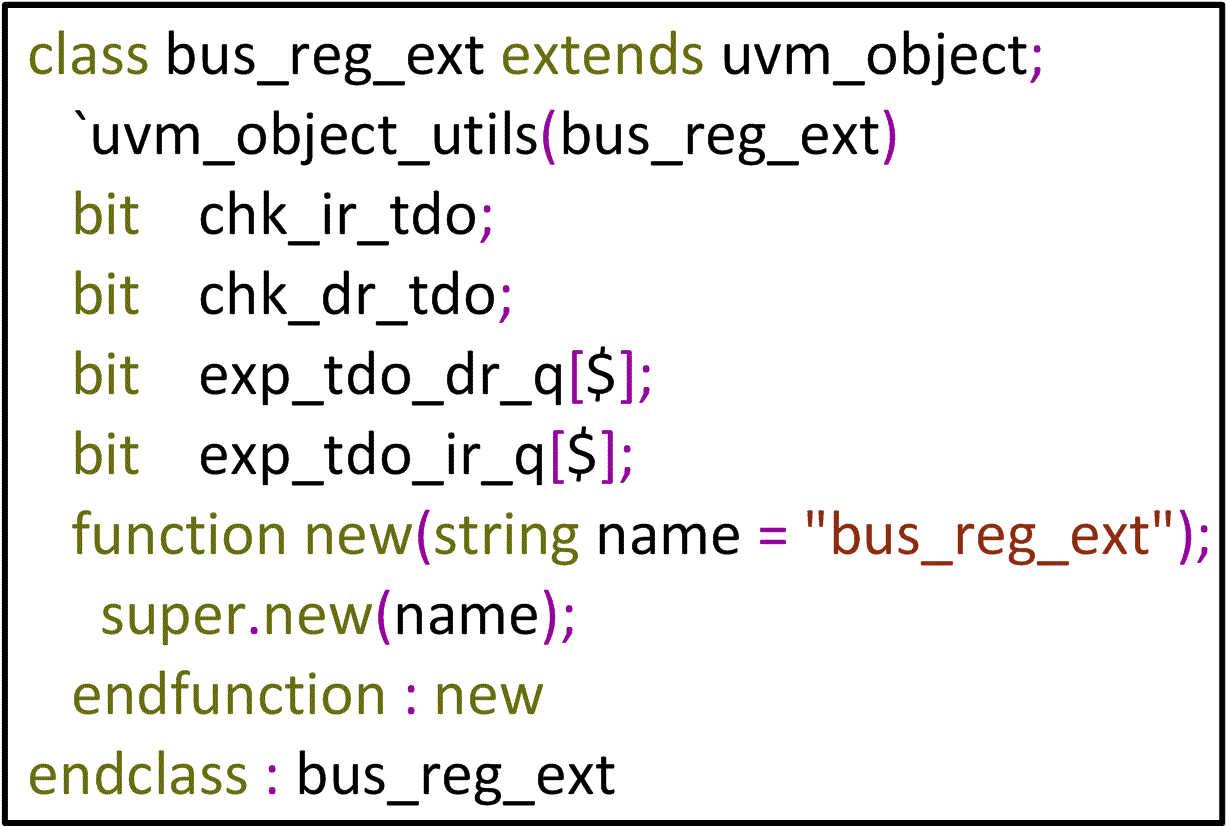


Figure 21. ***bus\_reg\_ext*** properties definition.

# IV. STIL Test Pattern Verification

In order to verify the content and behaviours of the generated STIL file, we can use STIL VerifyTM to generate a Verilog testbench and re-run simulation before delivering to ATE test engineers. The STIL file is verified if the simulation passes.

STIL VerifyTM is a free verification utility provided by Mentor Graphics for checking the conformity of STIL files, which ensures that STIL files are syntactically correct, and features a Verilog testbench that allows EDA (Electronic Design Automation) and ATE tool developers to run and display STIL content in any Verilog simulator taking STIL file and DUT as input [4].

# V. Discussion

In Figure 1, ***pad\_agent*** is mostly a physical layer agent that only toggles and samples pads directed by ***pad\_rw\_transaction***s, and has no knowledge about interface protocols, although it groups pads based on their interface protocols. If needed, the user can implement an upper layer agent to convert protocol-related transactions to ***pad\_info\_transaction***s and pass them down to ***pad\_agent***.

For the sake of simplification, this paper focuses on describing how to build a verification environment that can convert UVM tests to test patterns for ATE test during simulation, and the common components such as coverage collectors and scoreboards are not shown, the user can easily implement them using sequence items coming from ***jtag\_monitor***, ***dft\_tdr\_monitor*** and ***pad\_monitor***.

Fig. 21 is an example of building an upper layer agent that includs a scoreboard and a coverage collector using sequence items from ***pad\_monitor***, above the pad\_agent. Inside ***scan\_agnet***, scan related protocols are implemented in ***scan\_trans\_to\_pad\_rw\_trans\_sequence*** which converts each ***scan\_transaction*** to a serial of ***pad\_rw\_transaction***s. ***scan\_monitor*** collects ***pad\_rw\_transaction***s and converts them into ***scan\_transaction***s.

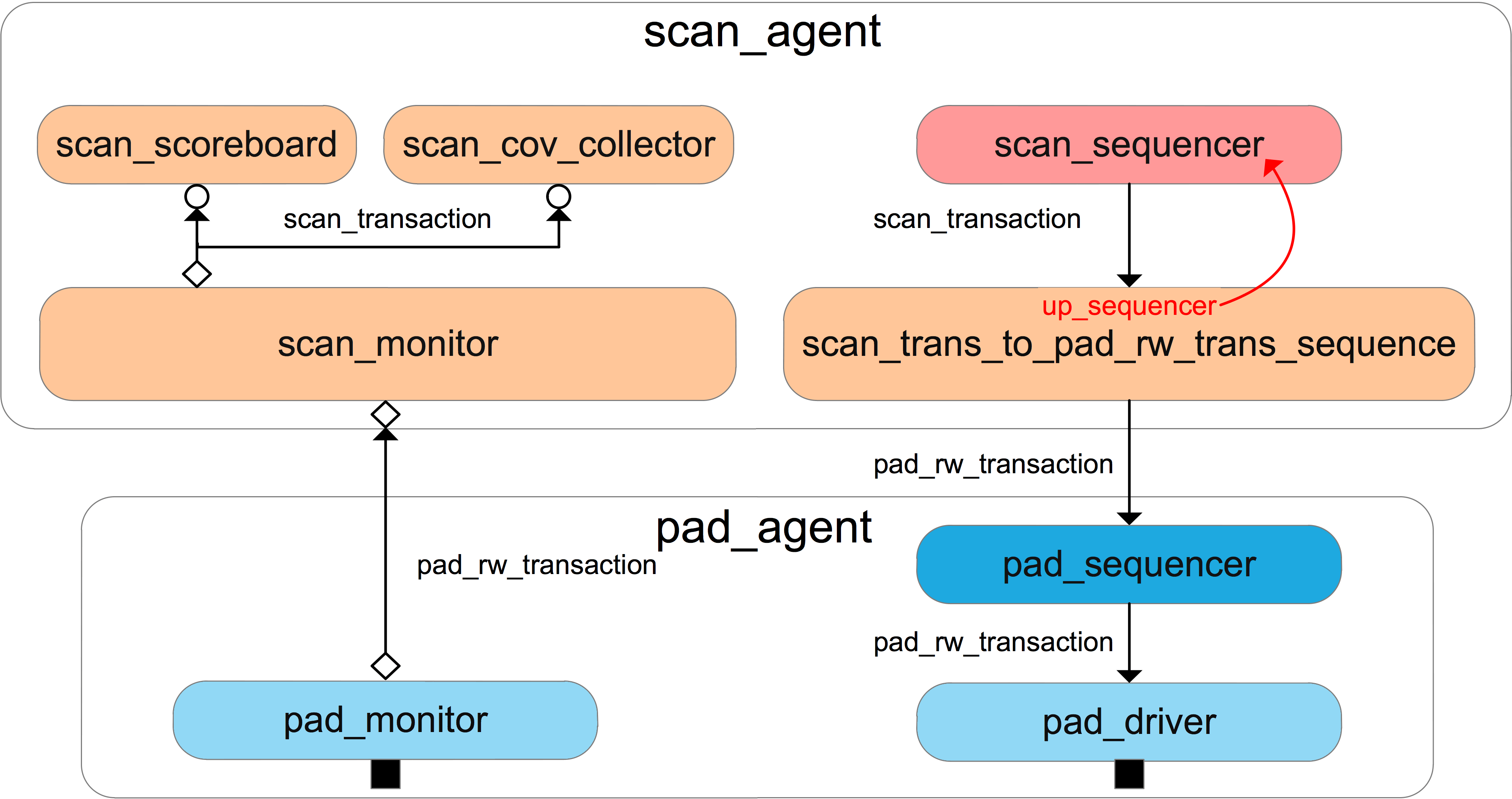


Figure 22. An example of building upper layer agent above ***pad\_agent***

Because we enforce every pad drive and sample should be done by a driver except for reference clock pads and each driver passes STIL information to the ***STIL\_generator*** whenever it drivers and samples a pad, the generated STIL pattern is functionally equivalent to its corresponding UVM test. Coverage statistics, which is gathered from coverage collectors to rank a UVM test, is also used to rate the generaged STIL pattern.

# VI. Conclusion

This UVM-based DFT environment can be easily adopted in most projects for DFT function verification by overriding ***dft\_env\_configuration***, grouping pads as shown in Section B, and defining related interfaces.

By modifying the ***call\_stil\_gen*** () method in each driver to transfer pad toggle and measurement information to the format of the other test language required, this environment could also generate other format patterns ATE needs, not just the STIL format.

Using this method, it saves usually a team’s work to translate DFT function tests to STIL patterns in a project, and more important, it avoids errors introduced in the muanul translation process to save turnaround debug efforts.

The approach to lift TDR in RAL is also a general way and can be applied in most projects by modelling related ***dft\_tdr\_network*** and overriding ***dft\_tdr\_trans\_to\_jtag\_trans\_sequence***. And it makes it easy to migrate UVM tests developing from this UVM-based DFT verification environment among verification environments and tests from block to system levels.

This UVM-based DFT environment works correctly in an experiment project and the generated STIL test pattern files pass simulation using STIL VerifyTM, which indicates it could be applied in real projects.

The next step is to use this environment in real projects and validate it in post-silicon debug.

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